Jarkko **Huijts**

Hardware engineer with over 10 years of experience

☏ +31 647185722 • ✉ jarkko.huijts@gmail.com
Dutch • male • 37 • Eindhoven, Netherlands

SKILLS AND EXPERIENCE

Hardware design	For ASIC and FPGA; VHDL, (System)Verilog, UVM, SystemC; verification, validation; documentation; clock-domain crossing (CDC), constraints, DfT, low-power design
Designed/implemented	VLIW DSP, debug support, Viterbi, SHA, DMA, FIFOs, asynchronous bridges, AMBA and proprietary bus components; SoC integration
Used/adapted IPs	ARM, LEON2, microcontrollers; processor and interface peripherals, memory controllers (DDR, NOR, NAND, SD), LCD touchscreen, ADCs, PMUs, audio codecs
Programming	C, C#, among others; Tcl, Perl, Python, Excel (VBA), MATLAB; boot loaders, drivers (bare metal, Linux); validation utilities, test equipment automation
EDA tools	Various tools from Synopsys, Cadence, Mentor and Xilinx for simulation, synthesis, equivalence checking, ATPG, CDC verification
Tools/flows	Integration with Magillem/SystemIntegrator; familiar with NXP and Freescale tools and flows; version control: Git, Mercurial, SVN, DesignSync; Linux user since 1997

EMPLOYMENT HISTORY

04/2016 – present — **NXP, via TMC** (Eindhoven)
- Integrated SoC for secure CAN
- Integrated Ethernet switch SoC
- Automated integration and documentation flow

05/2015 – 03/2016 — **Holst Centre (IMEC), via TMC** (Eindhoven)
- Designed, verified and validated Bluetooth LE signal detector
- Automated validation
- Designed low-power Viterbi decoder

03/2009 – 04/2015 — **Recore systems** (Enschede)
- Taped out a multicore DAB radio SoC
- SoC integration for ESA (European Space Agency)
- Designed debug support for a VLIW DSP
- Created IP database and scripts for hardware design

11/2008 – 01/2009 — **Centric TSolve** (Ulm, Germany)
- Taken measurements on prototype mobile phones
- The office closed down in 2009

01/2008 – 10/2008 — **Recore systems** (Enschede)
- Implemented a VLIW DSP

EDUCATION AND TRAINING

11/2018 — **IMEC** (Leuven, Belgium)
Course: Advanced digital physical implementation flow

02/2011	**Synopsys** (Reading, England) Course: Design Compiler 1
09/2000 – 12/2007	**University of Twente** (Enschede) Master's degree in computer science (MSc) Major: embedded systems Minor: electrical engineering Thesis topic: DfT, manufacturing testing

LANGUAGE ABILITIES

Dutch	mother tongue
English	fluent
German	advanced