

Jarkko Huijts

Hardware engineer with 7 years of experience

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Dutch • male • 32 • Enschede, Netherlands

SKILLS AND EXPERIENCE

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| Hardware design | For ASIC and FPGA; VHDL, Verilog, SystemC; verification (incl. post-layout), validation; documentation; clock-domain crossing, low-power design, DFT |
| Designed/implemented | VLIW DSP, debug support, DMA, FIFOs, asynchronous bridges, AMBA and proprietary bus components; SoC integration |
| Used/adapted IPs | LEON2, ARM926, many processor and interface peripherals, memory controllers (DDR, NOR, NAND, SD), LCD touchscreen, PMUs, audio codecs, ADCs, NoC; Microchip microcontrollers |
| Programming | C, C++, assembly (various), Tcl, among others; drivers (bare metal, Linux), boot loaders, validation utilities |
| Tools/software | Synopsys: DC, TetraMax, Formality; Mentor: QuestaSim, Precision; Xilinx: ISE; version control: Mercurial, Git; Linux user since 1997 |

EMPLOYMENT HISTORY

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|-------------------|---|
| 03/2009 – present | Recore systems (Enschede), hardware engineer <ul style="list-style-type: none">• Taped out a multicore DAB radio SoC• Integrated a SoC for the European Space Agency• Designed debug support for a VLIW DSP• Created fixed-function DSPs• Created IP database and scripts for hardware design• Defined VHDL coding standard |
| 11/2008 – 01/2009 | Centric TSolve (Ulm, Germany), hardware test engineer <ul style="list-style-type: none">• Taken measurements on prototype mobile phones• The office closed down in 2009 |
| 01/2008 – 10/2008 | Recore systems (Enschede), hardware engineer <ul style="list-style-type: none">• Implemented a VLIW DSP• Implemented DFT improvements |

EDUCATION

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| 09/2000 – 12/2007 | University of Twente (Enschede) Master's degree in computer science (MSc) Major: embedded systems, minor: electrical engineering |
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LANGUAGE ABILITIES

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| Dutch | mother tongue |
| English | fluent |
| German | advanced |
| French, Japanese | basic |